ABSTRACT

The invention relates to the design of highly reliable microprocessors and more specifically to the use of a dedicated state machine that periodically checks the validity of critical processor resources. In an embodiment of the present invention, an apparatus to detect errors in information stored in a processor resource includes an error detection component, which is configured to control the detection of errors in the information stored in the processor resource; and a comparison component coupled to the error detection component, which is configured to receive the information from the processor resource and inputs from the detection component. The comparison component is further configured to determine if the information is valid, and to output a signal to replace the information if the information if invalid.